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RFSA2724

Serial Controlled Digital Step Attenuator, 50MHz to 4000MHz

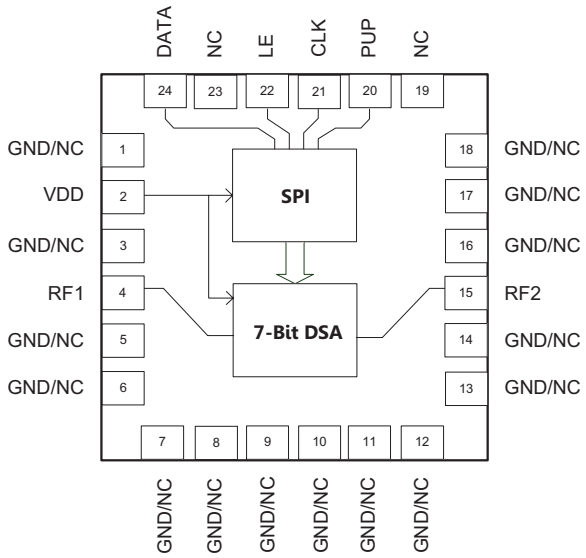
Package: MCM, 24-Pin, 4.2mm x 4.2mm

Features

- Frequency Range 50MHz to 4000MHz
- 7-Bit, 31.75dB Range, 0.25dB Step
- High Linearity, IP3 > 50dBm
- 3V and 5V Logic Compatible
- Serial-to-Parallel Controller
- Serial Programming Interface
- Power-up Programming Modes
- On-chip ESD Protection Class 2 < 4000V
- Single Supply, 3V to 5V Operation
- Footprint Compatible with Most 24-Pin, 4mm x 4mm QFNs

Applications

- Transceiver IF Applications
- Cellular, PCS, GSM, UMTS, LTE,
- WiMax/WiFi
- Wireless Data, Satellite Terminals
- Test Equipment



Functional Block Diagram

Product Description

RFMD's RFSA2724 is a 7-bit digital step attenuator (DSA) that features high-linearity over the entire 31.75dB gain control range with excellent step accuracy in 0.25dB steps. The RFSA2724 is programmed via a serial mode control interface that is both 3V and 5V compatible. The RFSA2724 also offers a rugged Class 1B HBM ESD rating via on-chip ESD circuitry. The MCM package is footprint compatible with most 24-pin 4mm x 4mm QFN packages.

Ordering Information

RFSA2724SR	7” Sample reel with 100 pieces
RFSA2724SQ	Sample bag with 25 pieces
RFSA2724TR13	13” Reel with 2500 pieces
RFSA2724PCK-410	50MHz to 4GHz PCBA with 5-piece sample bag

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	+5.5	V
DC Supply Current	15	mA
Power Dissipation	83	mW
Max RF Input Power	27	dBm
Operating Temperature (T_{CASE})	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Junction Temperature	150	°C
ESD Rating (HBM)	Class 2 (< 4000)	V
ESD Rating (CDM)	Class IV (> 1000)	V
Moisture Sensitivity Level	MSL3	

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Frequency Range	50		4000	MHz	
Insertion Loss		0.85 1.1 1.7 2.2		dB	150MHz, 0dB attenuation 850MHz, 0dB attenuation 2700MHz, 0dB attenuation 3800MHz, 0dB attenuation
Gain Control Range		31.75		dB	0.25dB step size
Step Accuracy		±(0.1 + 5.0% attenuation setting)		dB	
Input IP3		50		dBm	100MHz to 4000MHz
Input P0.1dB		25		dBm	1000MHz
Return Loss		15		dB	DC to 3500MHz, all states
Control Interface		7-bit, Serial			Serial Interface
Settling Time		200		ns	t_{RISE}, t_{FALL} (10%/90% RF)
Switching Speed		200		ns	t_{ON}, t_{OFF} (50% CTL to 10%/90% RF)
Supply Voltage (V_{DD})	4.75	5.0	5.25	V	
Supply Current		7.5		mA	
Control Voltage (V_{CTL})	Low, V_{CTL} = 0V to 0.8V High, V_{CTL} = 2.0 to V_{DD}			V	

Notes:
1. V_{DD} = 5V, V_{CTL} = 5V, T = 25 °C.
2. IIP3 measured with P_{IN} = +10dBm/tone, 1MHz spacing

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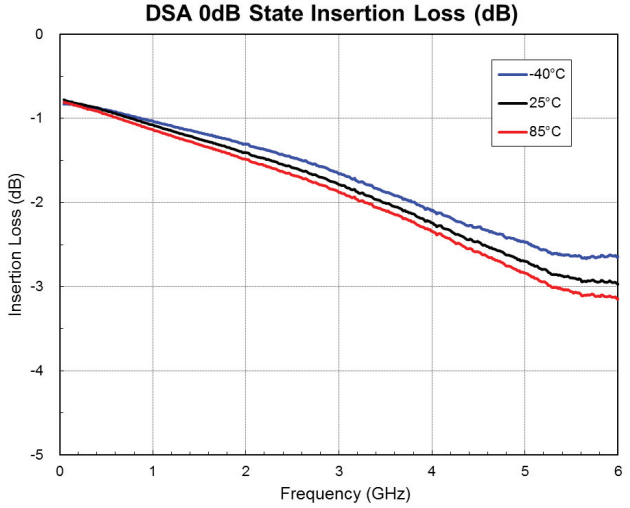
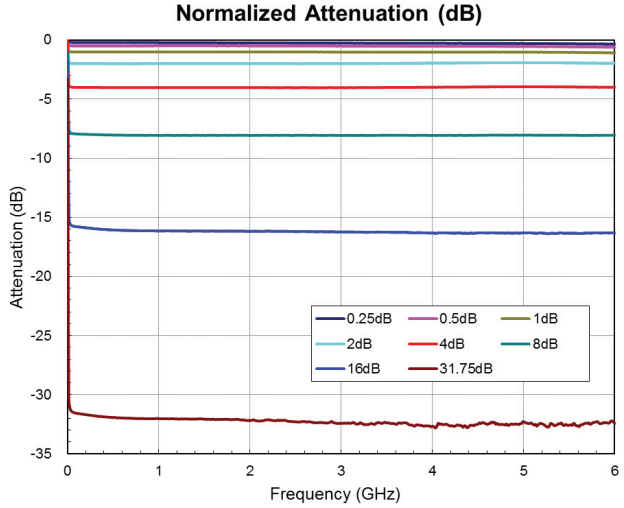
Typical Performance: Broadband Application Circuit (25°C)

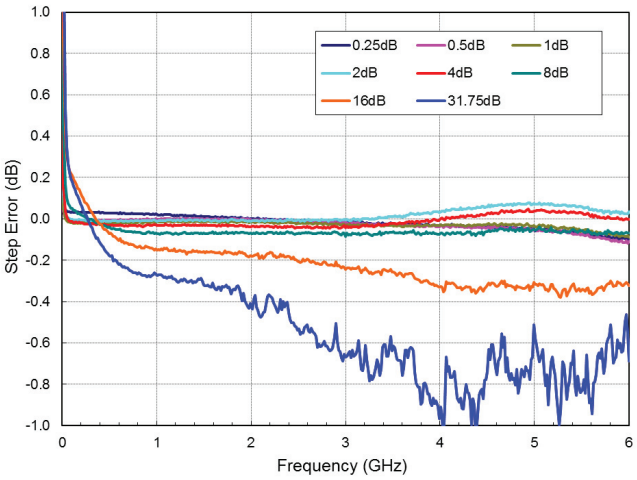
DSA 0dB State Insertion Loss (dB)



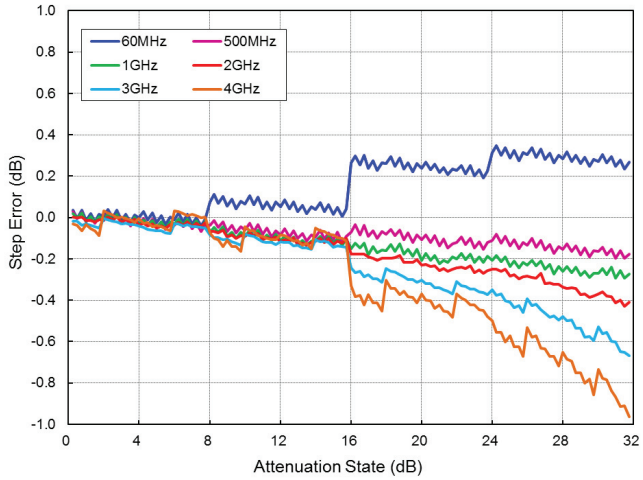
Normalized Attenuation (dB)



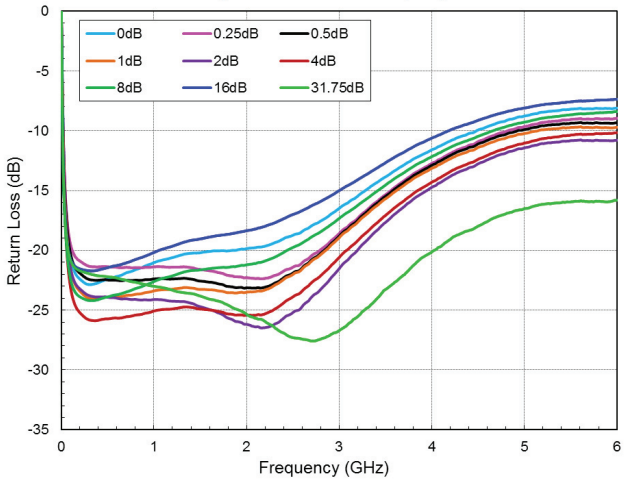
DSA Major Step Error (dB)



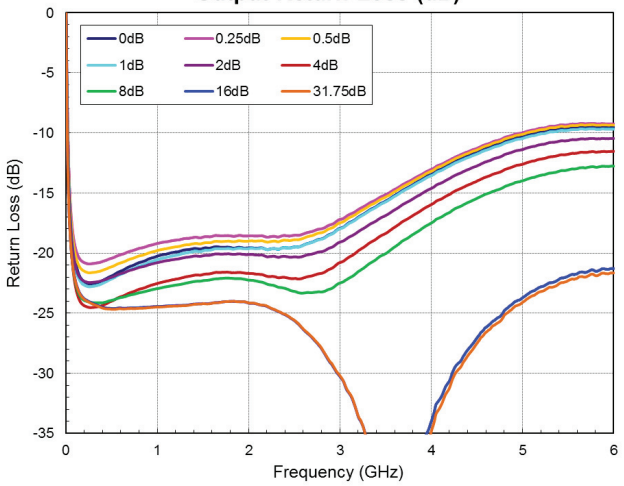
Step Error (dB)



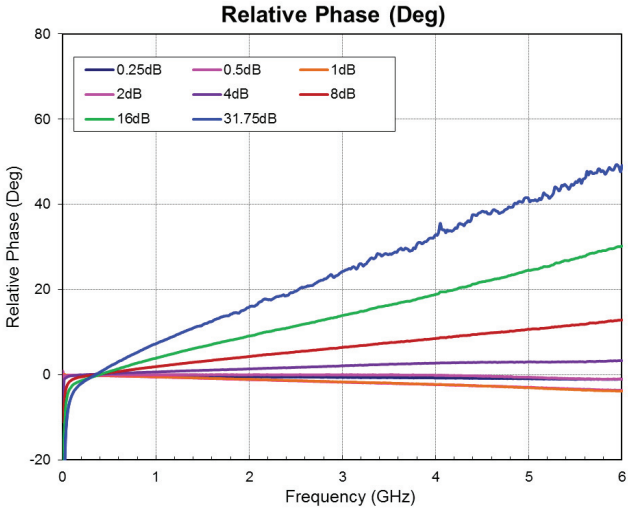
Input Return Loss (dB)

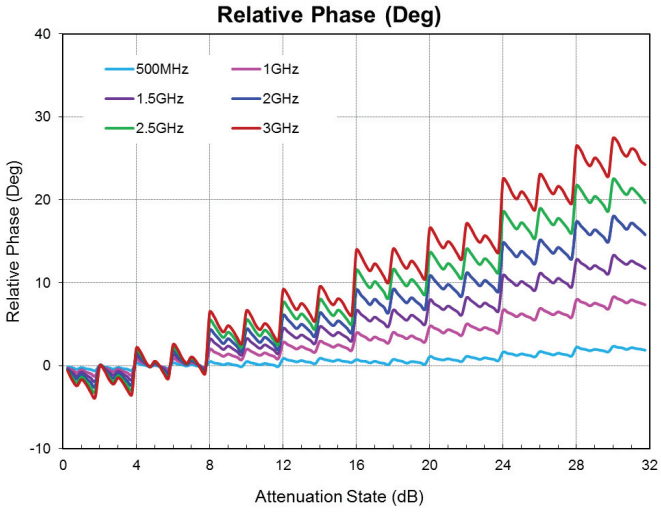


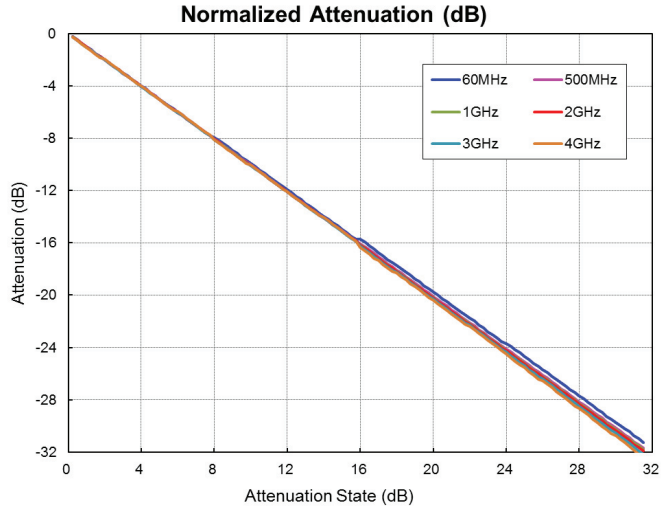
Output Return Loss (dB)

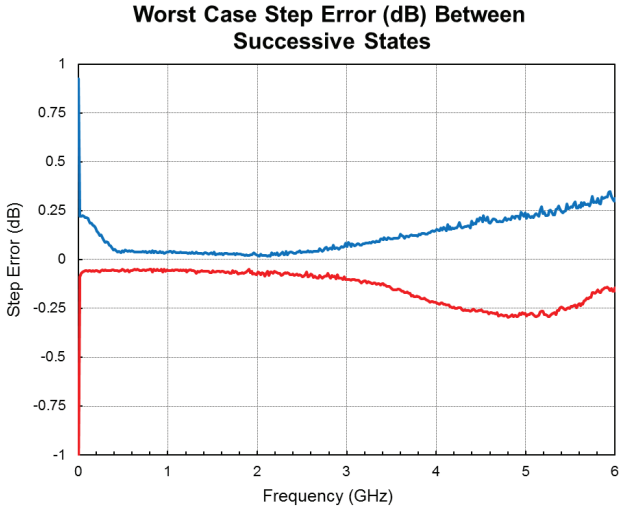


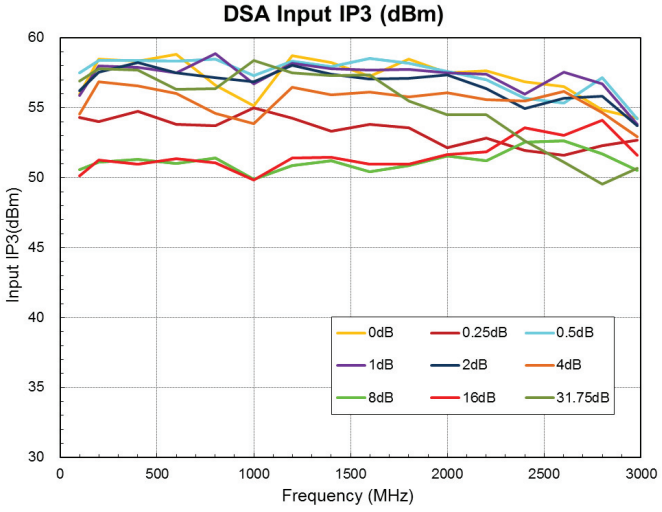
Typical Performance: Broadband Application Circuit (25 °C)











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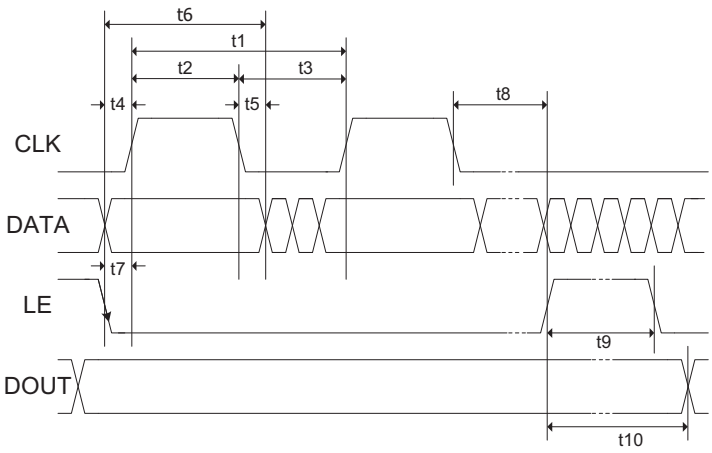
Truth Table

Control Bit							Relative Gain Setting
C16	C8	C4	C2	C1	C0.5	C0.25	
1	1	1	1	1	1	1	Max gain
1	1	1	1	1	1	0	-0.25dB
1	1	1	1	1	0	1	-0.5dB
1	1	1	1	0	1	1	-1dB
1	1	1	0	1	1	1	-2dB
1	1	0	1	1	1	1	-4dB
1	0	1	1	1	1	1	-8dB
0	1	1	1	1	1	1	-16dB
0	0	0	0	0	0	0	-31.75dB

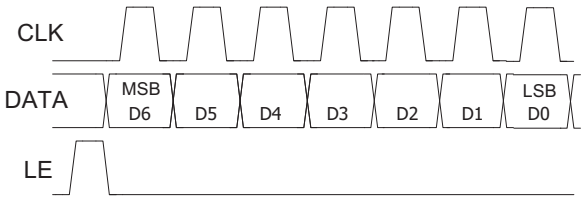
Note: C0.25 = D0, C0.5 = D1, ..., C16 = D6 (for the purpose of the example below)

Serial Port Interface

SPI Timing Diagram



Programming example – 7 bit



SPI Timing Diagram Specifications

Parameter	Limit	Unit	Comment
t1	25	MHz max	CLK Frequency
t2	20	ns min	CLK High
t3	20	ns min	CLK Low
t4	5	ns min	DATA to CLK Setup Time
t5	5	ns min	DATA to CLK Hold Time
t6	30	ns min	DATA Valid
t7	5	ns min	LE to CLK Setup Time
t8	5	ns min	CLK to LE Setup Time
t9	10	ns min	LE Pulse Width
t10	20	ns max	Output Set

Logic Voltage Levels	
State	Logic
Low	0V to 0.8V
High	2.0V to 5.0V

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Pin Names and Description

Pin	Function	Description
1	NC	No Internal Connection. EVB can be ground or no connect.
2	VDD	Power Supply.
3	GND	DC and RF Ground.
4	RF1	RF Port. External DC Block Required.
5	GND	DC and RF Ground.
6	GND	DC and RF Ground.
7	GND	DC and RF Ground.
8	GND	DC and RF Ground.
9	GND	DC and RF Ground.
10	GND	DC and RF Ground.
11	GND	DC and RF Ground.
12	GND	DC and RF Ground.
13	GND	DC and RF Ground.
14	GND	DC and RF Ground.
15	RF2	RF Port. External DC Block Required.
16	GND	DC and RF Ground.
17	GND	DC and RF Ground.
18	GND	DC and RF Ground.
19	NC	No Internal Connection. EVB can be ground or no connect.
20	PUP	Power-up Programming Pin. Low = Max Attenuation (31.75dB) at power-up. High = Min Attenuation (0dB) at power-up.
21	CLK	Serial Clock.
22	LE	Latch Enable.
23	NC	No Internal Connection. EVB can be ground or no connect.
24	DATA	Serial Data.
EPAD	GND	DC and RF Ground. Must be soldered to EVB ground plane over a bed of vias for thermal and RF performance.

Power-up Programming Truth Table	
PUP	Attenuator Setting
Low	Attenuation at Max, 31.75dB
High	Attenuation at Min, 0dB

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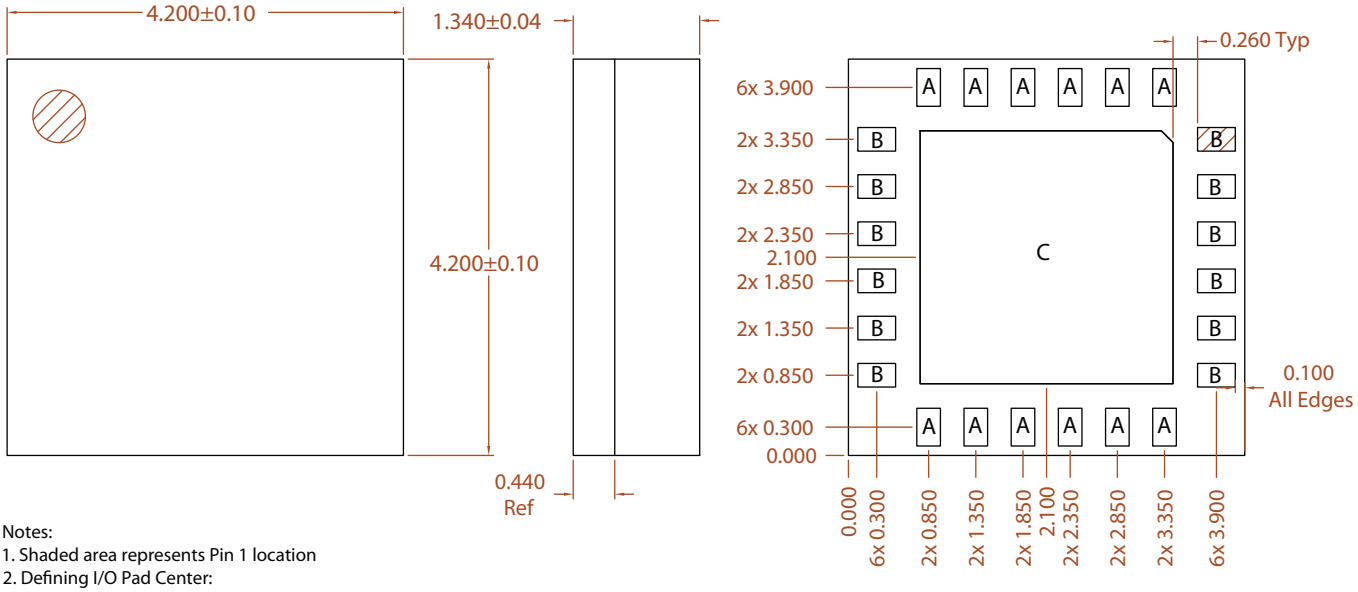
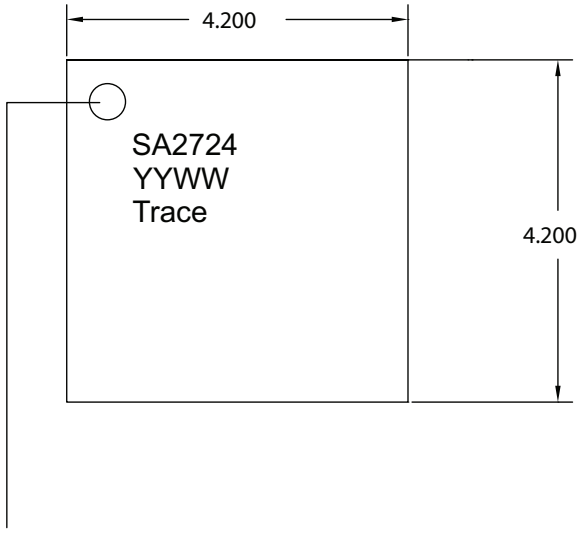
Package Outline Drawing



Notes:
1. Shaded area represents Pin 1 location
2. Defining I/O Pad Center:
   To define center of the I/O pad opening, draw a right triangle in one corner of the I/O pad
   Then take the center of the hypotenuse to determine center of I/O pad

A = 0.250 x 0.400 mm Typ
B = 0.400 x 0.250 mm Typ
C = 2.680 x 2.680 mm

Branding Diagram

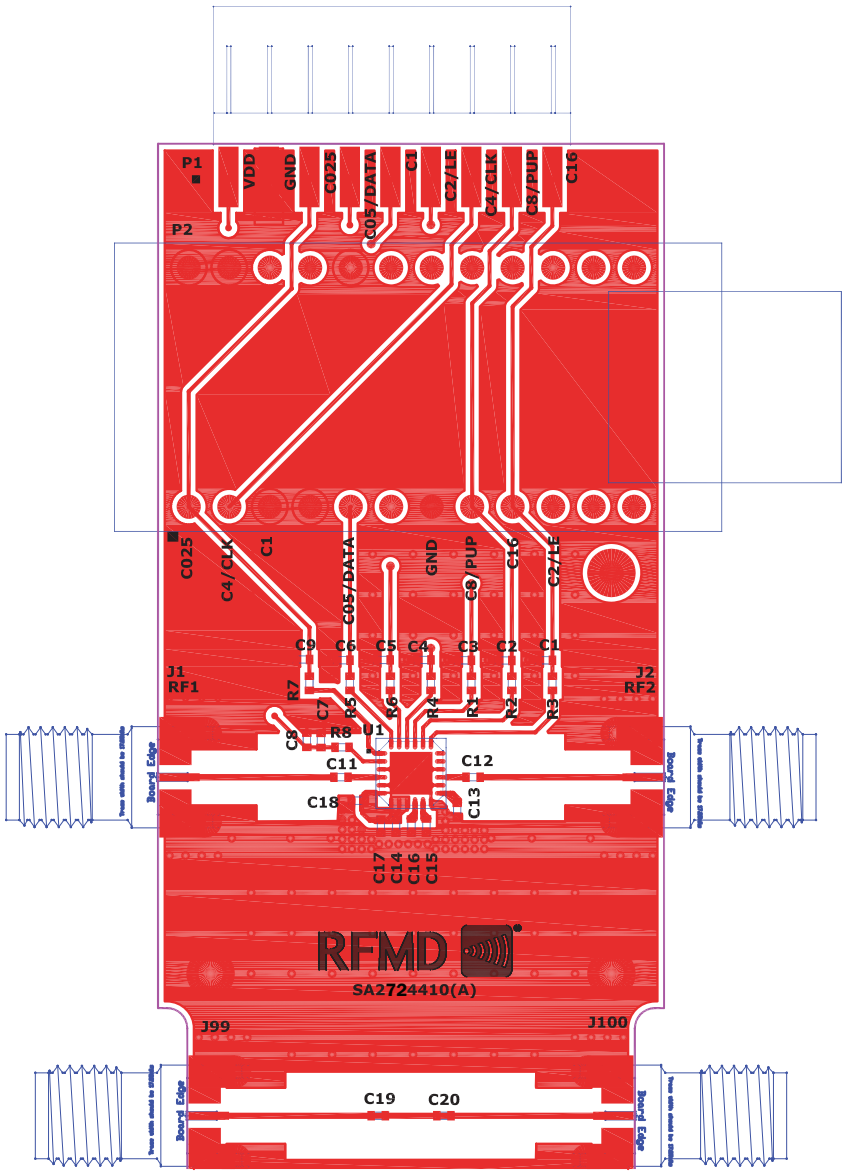


Pin 1 Indicator

Fill in the YYWW Notation with the Date Code
YY = Year
WW = Week

Trace to be assigned by SubCon

Evaluation Board Assembly Drawing



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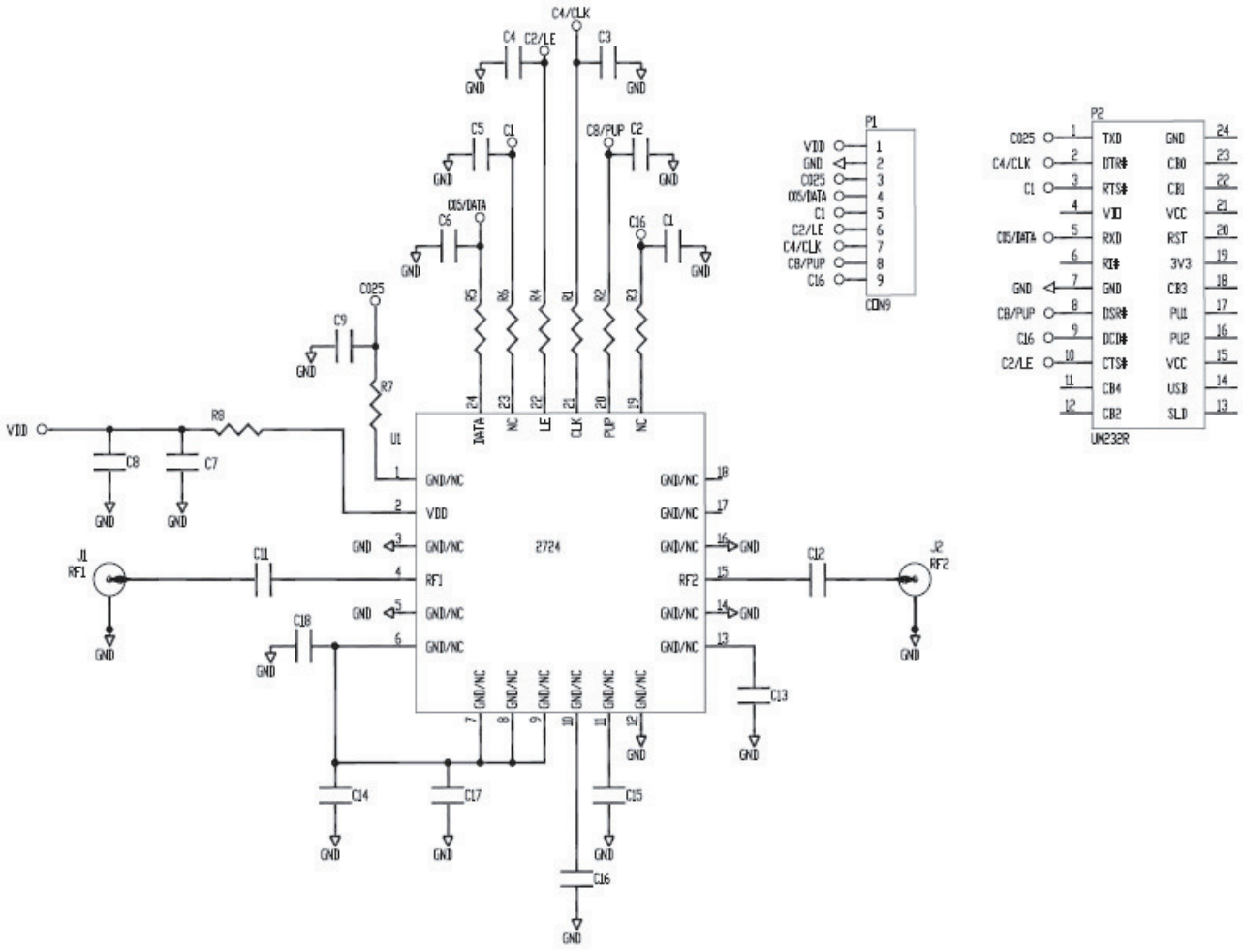
Evaluation Board Schematic



Evaluation Board Bill of Materials (BOM)

Description	Reference Designator	Manufacturer	Manufacturer's P/N
SA2714410(A)		Dynamic Details (DDI) Toronto	SA2714410(A)
Digital Step Attenuator 50MHz to 4000MHz	U1	RFMD	RFSA2724SB
CAP, 470pF, 10%, 50V, X7R, 0402	C11-C12	Murata Electronics	GRM155R71H471KA01E
CAP, 1000pF, 10%, 50V, X7R, 0402	C7	Taiyo Yuden (USA), Inc.	RM UMK105BJ102KV-F
RES, 0Ω, 0402	R1-R2, R4-R5, R8	Kamaya, Inc	RMC1/16SJPTH
CONN, SMA, END LNCH, UNIV, HYB MNT, FLT	J1-J2, J99-J100	Molex	SD-73251-4000
CONN, HDR, ST, PLRZD, 9-PIN	P1	ITW Pancon	MPSS100-9-C
CONN, SKT, 24-PIN DIP, .600", T/H	P2	Aries Electronics Inc.	24-6518-10
MOD, USB TO SERIAL UART, SSOP-28	M1 (See Note Below)	Future Technology Devices Int'l	UM232R
DNP	C1-C6, C8-C9, C13-C20	NA	NA
DNP	R3, R6-R7	NA	NA

Note: M1 should be mounted into P2 with respect to the Pin 1 alignment of M1 and P2